In the Specification:

Please replace the paragraph beginning on page 10, line 26 with the following amended paragraph:

The luminance inclination circuit 1 is constituted of three resistances R5, R6, R7, two n-channel transistors (FETs) NT3, NT4, and one p-channel transistor (FET) PT2. Further, since a voltage fluctuation in synchronization with the outputs VOUTi of the gate driving circuit 4 is required, a gate clock signal GCLK for shifting the outputs VOUTi of the gate driving circuit 4 and a luminance inclination circuit control signal XGCLK that is inverted from the gate clock signal GCLK are inputted to the luminance inclination circuit 1. Incidentally, the gate clock signal GCLK and the luminance inclination circuit control signal XGCLK are generated in a ~~later-descried~~ later-described timing generating circuit.